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# Controlling Power Up and Power Down of the Synchronous MOSFETs in a Half-Bridge Converter

by

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## ABSTRACT

The half-bridge converter has several major advantages over other topologies, but in the past it also had the disadvantage of providing no way for the designer to control the secondary synchronous MOSFETs during dwell time or to predict when they need to turn off. This paper outlines the problems associated with driving the synchronous MOSFETs using generic half-bridge controllers and demonstrates how they were overcome by the introduction of a primary side half-bridge controller that incorporated the driving the logic for the synchronous MOSFETs. However, even with this controller and the correct logic signal outputs, there remained a requirement for application circuits to handle start-up and shut-down, due to the need for the secondary side synchronous MOSFETs to be on when the primary MOSFETs are off. If not managed correctly the MOSFETs being inherently on can cause undesirable conditions during start-up and shutdown. This paper describes a new integrated circuit that has been developed to control the synchronous MOSFETs during start-up and shutdown, even under pre-biased conditions.

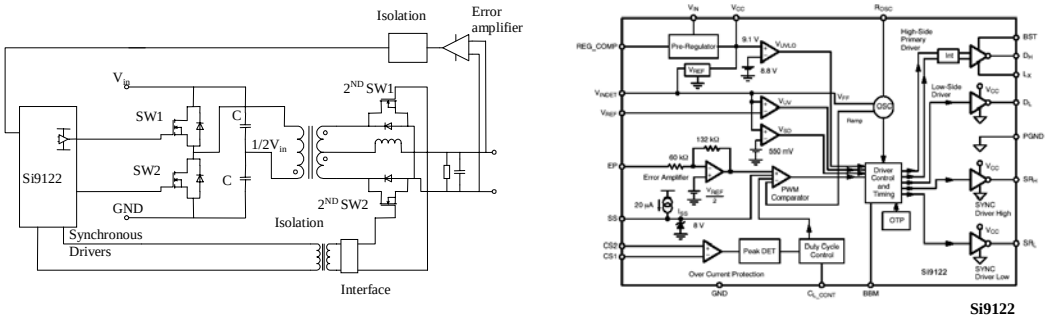
This paper will demonstrate how the half-bridge converter can be implemented with two ICs (one primary and one secondary) to provide an alternative to existing topologies in small, efficient, dc-to-dc converters. It shows that the problems of the past, which may have prevented designers from using this topology, can be overcome.

## INTRODUCTION - THE HALF-BRIDGE DC-DC CONVERTER

The half-bridge dc-to-dc converter configuration consists of two large, equal capacitors connected in series across the dc input, providing a constant potential of ½ $V_{in}$ at their junction, as shown in Figure 1a[1]. The MOSFET switches SW1 and SW2 are turned on alternatively and are subjected to a voltage stress equal to that of the input voltage, rather than twice the input voltage which is usually the case in push-pull and forward converters. Also, due to the capacitors providing a mid voltage point, the transformer sees a positive and negative voltage during switching. This results in twice the desired peak flux value of the core, since the transformer core is operated in the first and third quadrant off the B-H loop, and it experiences twice the flux excursion of a similar forward converter core.

An advantage of the half-bridge topology, over that of double-ended forward topologies, is that the half-bridge primary transformer winding has half the turns for the same input voltage and power. This is because the forward converter must sustain the full supply voltage, compared to half that voltage for the half bridge. Another benefit of half bridges is lower winding costs and lower proximity effect losses. Proximity effect losses occur when eddy currents are induced in one winding layer by currents in adjacent layers. These losses increase significantly with the number of layers. Because the half-bridge converter has fewer turns than the forward topology, then it probably will have fewer layers, and thus lower proximity effect losses.

Another significant advantage of the half-bridge over the double-ended forward converter is that the half-bridge secondary produces a full-wave output rather than a half-wave output. Thus the square-wave frequency in the half-bridge converter is twice that of the forward converter, and the associated output inductor and capacitor can be smaller.




a) b)[2]

**Figure 1. Block diagram of half-bridge topology and Si9122 IC.**

## PRINCIPLES OF OPERATION OF THE CONTROLLER IC (Si9122)

To fully understand the need for an intelligent driver in the half-bridge topology, it is necessary to describe the operation of the primary controller. This paper briefly describes the Si9122 (block diagram in Figure 1b), but full details can be found in the datasheet[2].

### Start up and soft start control.

Since the controller IC has a 75-V depletion mode technology, the full input voltage can be applied directly to the $V_{in}$ pin. The controller supply ($V_{cc}$) is derived from the input voltage via a pre-regulator circuit as shown in Figure 1. This is a linear regulator, and it regulates the input voltage to a target voltage of $V_{reg}$. Current into the external $V_{cc}$ reservoir capacitor is limited by the pre-regulator to typical level of 20 mA. When $V_{cc}$ exceeds the undervoltage lockout threshold ($V_{uvlo}$) of 8.8 V, a soft-start cycle of the switchmode supply is initiated. The $V_{cc}$ supply continues to be charged by the pre-regulator until $V_{cc}$ equals $V_{reg}$. During this period, between $V_{uvlo}$ and $V_{reg}$, an excessive load will result in $V_{cc}$ falling below $V_{uvlo}$ and stopping switchmode operation. This situation is avoided by the use of hysteresis between $V_{reg}$ and $V_{uvlo}$ and correct sizing of the reservoir bootstrap and soft-start capacitors. The value of the reservoir capacitor should therefore be chosen to be capable of maintaining switchmode operation until $V_{cc}$ is supplied from the output. Feedback from the output of the switchmode supply charges $V_{cc}$ above $V_{reg}$ and fully

disconnects the linear pre-regulator, isolating $V_{cc}$ from $V_{in}$. $V_{cc}$ is then maintained above $V_{reg}$ for the duration of switchmode operation.

Once $V_{cc}$ is greater than $V_{uvlo}$, the soft-start function is initiated and the switching pulse width is increased linearly from the minimum duty cycle ($D_{min}$) to maximum duty cycle ($D_{max}$). Under normal operation, if the controller IC identifies a low-voltage input, via the $V_{indet}$ pin, then the controller IC will be powered down. Once the input voltage recovers, the controller IC will again be powered up under soft-start control.

**Voltage mode and feed forward control**

The controller is designed to operate under voltage-mode control of pulse width modulation, at a fixed frequency. Duty cycle is controlled over a wide range to maintain output voltage under line and load variation. The signal from the isolated error amplifier is fed into the internal error amplifier via the $V_{ep}$ pin. Figure 2 shows the variation in duty cycle with respect to the voltage applied to the $V_{ep}$ connection.

A voltage feed forward scheme is included to take account of variations in the supply voltage $V_{in}$ and to provide a rapid transient response to line variation. The supply voltage is monitored, via a resistor divider, on the $V_{indet}$ pin of the IC. The variation in duty cycle attributable to the feed forward scheme, with respect to $V_{indet}$, is shown in Figure 3.

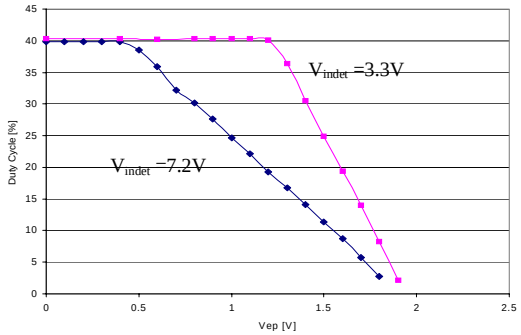



**Figure 2. Example of the voltage mode control.**

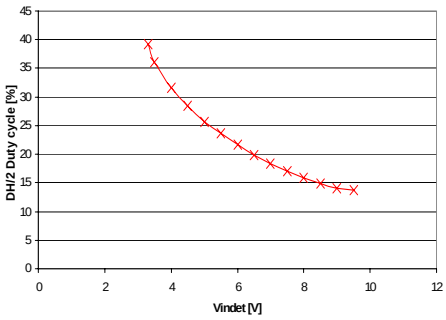



**Figure 3. Example of the voltage feed forward control.**

**Oscillator**

The oscillator is designed to operate at a frequency of 625 kHz nominal. The 625-kHz operating frequency allows a minimization of the inductor and capacitor sizes, improving the power density of the converter. The oscillator (and therefore the switching frequency) is programmable by attaching a resistor to the $R_{osc}$ pin.

**Break Before Make (BBM)**

The timing and synchronization of the drives to the primary and secondary stages are very important. It is essential to avoid the situation where both of the secondary MOSFETs are on when either the high- or low-side switches are active. In this situation, the transformer would effectively be presented with a short across the output. To avoid this outcome, a dedicated break-before-make circuit is included to ensure a non-overlapping waveform between the primary and the secondary drive

signals. This is achieved by a programmable timer which delays the switching of the primary driver at the beginning of the on period and delays the secondary driver at the end of the on period. The ideal switching waveforms are shown in Figure 4. It should be noted that the synchronous driver outputs from the controller IC are inverted to take into account the effect of the isolation circuit from the primary to the secondary side.

**Isolated drivers**

The controller IC includes an isolated driver to allow switching of the high-side primary switch without any additional buffers or isolation circuits. This is achieved by bootstrapping the $V_{cc}$ voltage onto the $L_x$ voltage, which is the high-side MOSFET's source terminal. To provide the bootstrapping, an external diode and capacitor are required, and the bootstrapping capacitor is charged up during the on time of the low-side device.

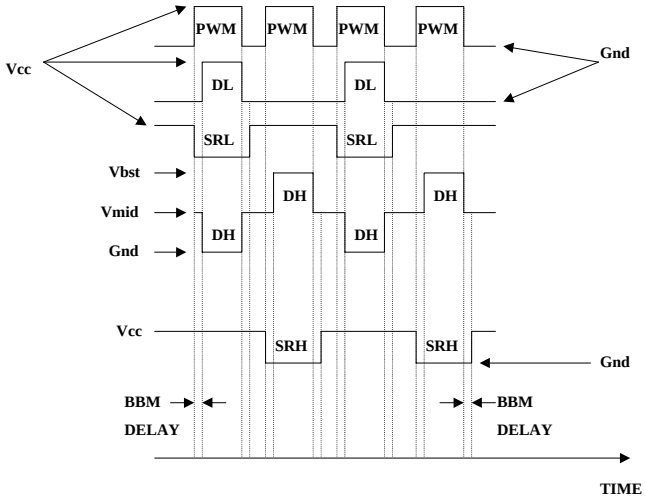



**Figure 4. BBM timing diagrams.**

**$V_{indet}$ threshold**

The chip provides a means of sensing the voltage of $V_{in}$, and withholding operation of the output drivers until a minimum voltage is achieved. This is achieved by choosing an appropriate resistive tap between the ground and $V_{in}$, and comparing this voltage with the reference voltage. When the applied voltage is greater than $V_{ref}$, the output drivers are activated as normal. $V_{indet}$ also provides the input to the voltage feed forward function.

**Overcurrent and overtemperature protection**

Current-mode control providing constant-current operation is achieved by monitoring the differential voltage between the CS1and CS2 pins, which are connected across a primary low-side sense resistor. Once this differential voltage exceeds the 100-mV trigger point, the PWM control of the output drive is taken over by the current limit control loop. This reduces the switching duty cycle. The rate at which this duty cycle decays is proportional to the excess voltage (above 100 mV) and the value of the external capacitor connected between the CL_CONT pin and ground. Once the duty cycle reduces to 12.5%, then any further reduction will be accompanied by a reduction in switching frequency at a rate proportional to the duty cycle. This prevents the on time of the primary drivers falling below 100 ns and hence avoids a current tail. Frequency reduction occurs to a maximum of one fifth of the nominal frequency. If the voltage between CS1 and CS2 exceeds 150 mV, the CL_CONT capacitor is discharged rapidly, resulting in minimum duty cycle and frequency immediately. Minimum duty cycle and reduced frequency switching continues for the duration of the fault condition. The converter reverts to voltage-mode operation immediately whenever the primary current fails to reach the 100-mV limit level.

**Shutdown**

If $V_{indet}$ is forced below the lower threshold, a minimum of 470 mV, the device will enter shutdown mode. This powers down all unnecessary functions of the controller, ensures that the primary switches are off, and results in a low-level current demand from the $V_{in}$ or $V_{cc}$ supplies of less than 200 µA.

**SECONDARY SIDE INTELLIGENT DRIVER**

The second integrated chip incorporates the majority of the external components required on the secondary side of an isolated half-bridge converter. The IC has an error amplifier, reference voltage, and synchronous rectifier drivers. As well as having these circuits, the driver enables controlled start-up and shutdown of the synchronous MOSFETs. Figure 5 shows a block diagram of the circuit.

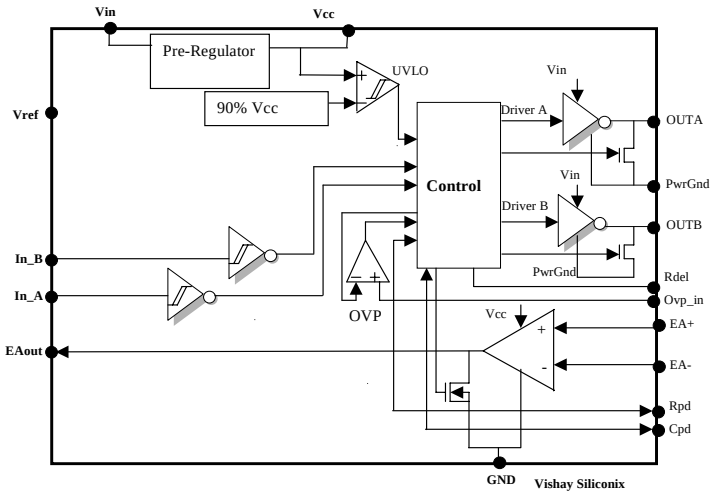



**Figure 5. Block diagram of the intelligent driver.**

**Powering the Intelligent Driver**

The IC has an in-built pre-regulator, which supplies the internal sub-circuits. The current into the external $V_{cc}$ capacitor is limited to typically 20 mA by this pre-regulator. Therefore the IC can be powered from any input voltage within the pre-regulator range of 5 V to 13 V. The gate drivers are supplied by $V_{in}$ and as such the gate voltage to the external MOSFETs can be set by the designers within the range of 5 V to 13 V. Setting the gate driver voltage ($V_{in}$) to 7.5 V allows a peak source drive capability of 2.5 A and a sink capability of 4 A.

The $V_{in}$ voltage can be derived from any of the usual methods such as an extra winding on the power transformer, or from the output inductor. However, in the circuit example prepared for this paper, the power is derived from the pulse transformer used to transmit the gate drive signals from the primary to the secondary, as shown in Figure 6.

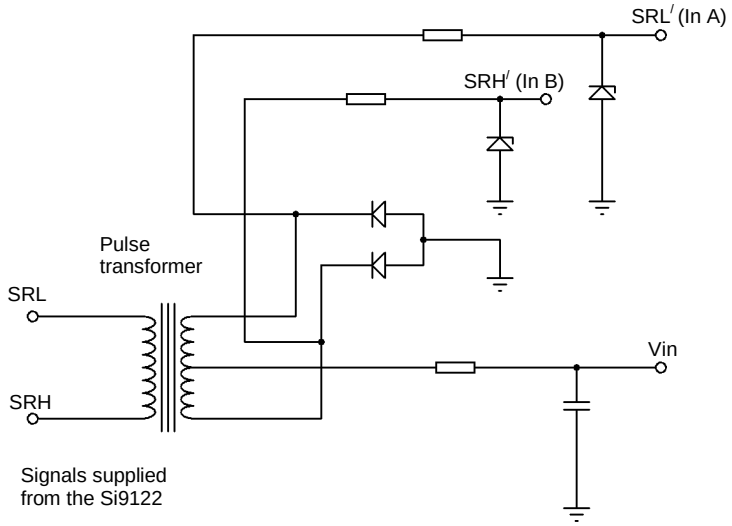



**Figure 6. Schematic showing powering intelligent driver from pulse transformer.**

**Normal Start-up of the Intelligent Driver – Output Drivers.**
During start-up of the converter and the intelligent driver, the MOSFET drivers initially need to be disabled, since the gate driver voltage could be at an indeterminable level, causing extra losses and even failures in the synchronous MOSFETs. Therefore the MOSFET drivers are disabled until $V_{cc}$ is at 90% of its final value.

If the output drivers were left floating until the main drivers were enabled, then the high dV/dt rate during the transition of the current from the SRL diode to the SRH diode (and vice versa) could result in spurious turn-on of the MOSFET. Therefore, before the main drivers are enabled ($V_{cc}$ <90%), the In-A and In-B drive paths are reversed (Figure 7), and there is a small driver on each output to pull the relevant gate driver outputs low at the appropriate time. For example, if high-side MOSFET (DH) on the primary side is turned on, then the body diode or Schottky diode associated with SRL MOSFET on the secondary side will start to conduct and the $V_{DS}$ across the MOSFET will fall to less than 1 V. Once DH is turned off, the current through the SRL diode will cease, and the voltage across the MOSFET will rise. It is during these transitions that the MOSFET could turn on, depending on $V_{th}$ levels and values of $C_{gd}$ and $C_{gs}$. During this time, SRH/ or In B is high, therefore this signal is used to drive a small inverting driver that keeps the SRL MOSFET off, even when the $V_{cc}$ has not been established. Once $V_{cc}$ is established, the small inverting driver is switched out of the path. Therefore the driver circuit will effectively hold the driver outputs low, until the $V_{cc}$ voltage level has reached 90% of its final value.

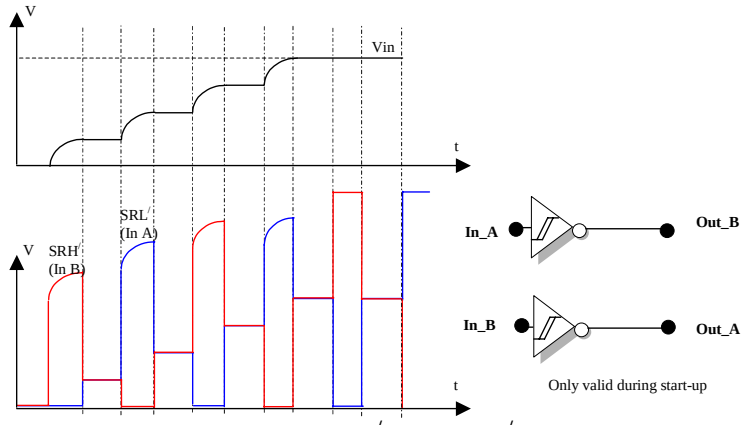



**Figure 7. Rise of Vin and SRL/ and SRH/ signals during start-up.**

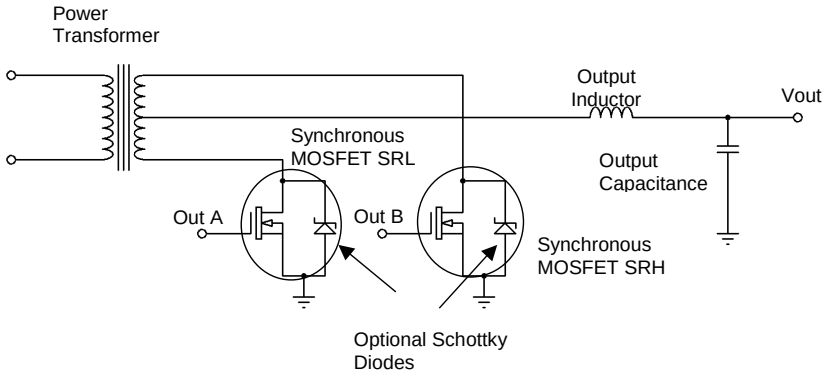



**Figure 8. Power stage of half-bridge converter**

**Normal Start-up of the Intelligent Driver – Vref.**

Once $V_{cc}$ has reached 90% of its final value, the external $V_{ref}$ is also released and able to rise according to the value of the $V_{ref}$ capacitor, as shown in Figure 9. The rate of rise of $V_{cc}$ is determined by the external $V_{cc}$ capacitor and the 20-mA pre-regulator current limit.

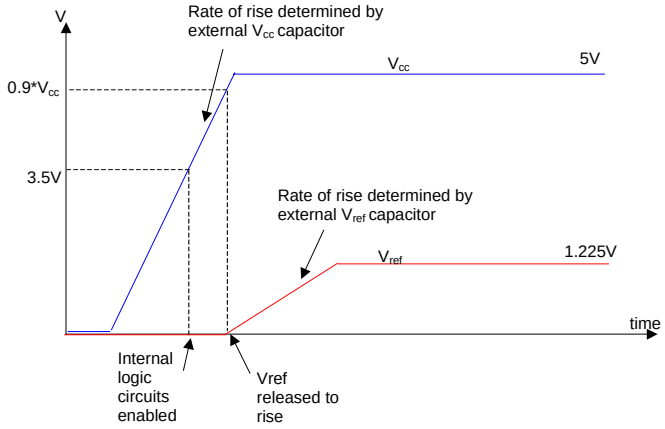



**Figure 9. Start-up Sequence.**

**Soft-Start of Output Drivers**

The start-up of the intelligent driver takes several cycles. Therefore it is possible for current to be conducted in the anti-parallel diode of the MOSFET, or, if Schottky MOSFETs are used, in the Schottky diodes. The voltage drop across the diodes is considerably larger than the level seen across the synchronous MOSFETs when they are conducting. The soft-start method, as shown in Figure 10, prevents disturbances in the output voltage. The soft-start period is set by an external resistor, and this also sets a single-edge delay to enable tuning of propagation delays in the system, as shown in Figure 11.

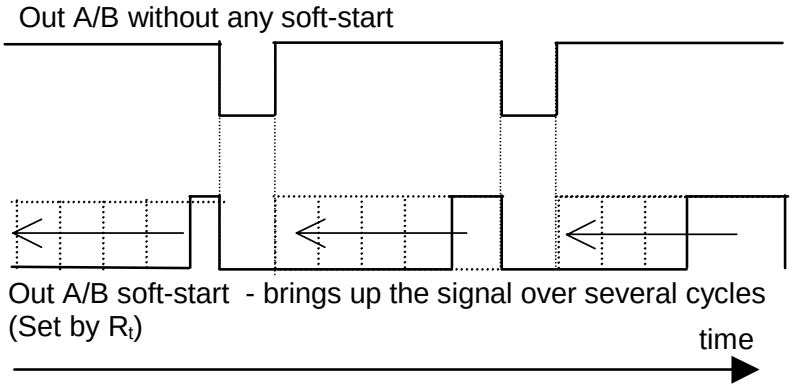



**Figure 10. Soft-start of the output drivers.**

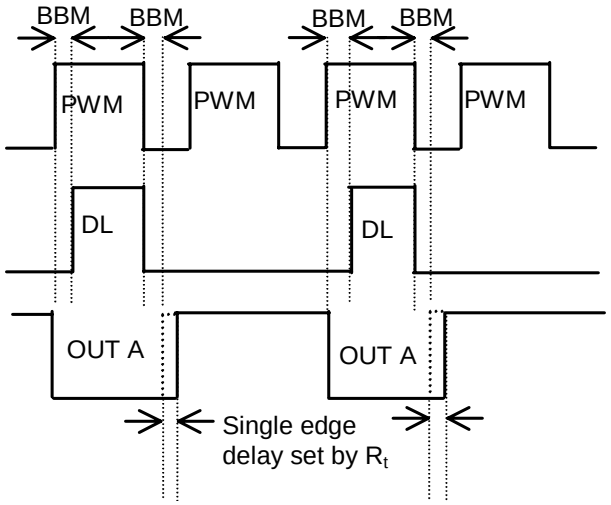



**Figure 11. Single edge delay set by an external resistor.**

**Overvoltage modes of operation.**

A separate pin is provided to detect overvoltage conditions, which can occur according to two separate modes. The first is an overvoltage during the start-up of the device. The second is an overvoltage during normal operation. An over voltage condition is defined as OVP_in being 20% greater than the final value of $V_{ref}$, which is approximately 1.4 V.

If an overvoltage occurs during start-up, the driver outputs are disabled until the external $V_{ref}$ has reached 90% of its final value of 1.225 V Once this occurs, the

output drivers are then released to respond to the input pulses. However if the overvoltage set point ($V_{ref}$+20%) is reached during normal operating conditions, or after $V_{ref}$ has reached 90% of its final value, then the overvoltage protection (OVP) comparator is latched and the output drivers are forced to the on condition. The external $V_{ref}$ is then discharged to 20% of its normal value. The output drivers are released when the overvoltage fault condition has cleared, which is defined as being 10% less than the final value of $V_{ref}$ (1.1 V). That is, the output drivers will stay on until $V_{ref}$ is discharged to 20% of the final value or the OVP_in is below 1.1 V (whichever is the longer). Once the output drivers are released the device will go through a soft-start condition.

**Normal Shutdown of the Intelligent Driver**

To prevent the synchronous MOSFETs staying on when the input pulses from INA and INB cease, this device has a function that discharges the gates of the synchronous MOSFETS before the bias supply to the IC disappears. The inputs are monitored, and when there is no activity on INA and INB after a certain time (set by $C_{PD}$ and $R_{PD}$), then the main drivers are disconnected and the driver outputs are discharged, under power-down control. The pull-down current will be a fixed ratio of the current set by an external resistor ($R_{PD}$) such that the discharge time can be a fixed number of pulses at the normal operating frequency. Without this function, no activity on the inputs of INA and INB (due to the primary side shutting down) would result in the synchronous MOSFETs staying on. Allowing the MOSFETs to remain on once the primary controller has been shut down can cause the output to be discharger and negative spikes can occur once the synchronous MOSFETs finally turn off.

## TEST RESULTS

Unfortunately due to time constraints the final test results were not completed in time for submission of this paper, however these will be presented at the conference and will be available as hand-outs. These will include load responses and efficiency results and will show the behavior of the circuit under the various modes and fault conditions described above.

## CONCLUSION

The primary controller IC has been demonstrated to provide the functional requirements for a half-bridge dc-to-dc converter with secondary synchronous rectification and initial measurements. The functionality of the sub-circuits within the controller have also been demonstrated, including the behavior of the error amplifier and the feed forward voltage scheme.

The paper shows that the controller IC, with its 625-kHz switching frequency and high level of integration, provides a very efficient, small, and robust dc-to-dc converter when implemented with the appropriate MOSFETs.

The secondary side intelligent driver, shown in Figure 12, incorporates the majority of components required in a half-bridge converter and also enables controlled start-up and shut-down, alleviating the need for the application circuits normally required with these topologies. Provided in an MLP44-16 pin package, the secondary-side intelligent driver will allow the use of high power density dc-to-dc converters.

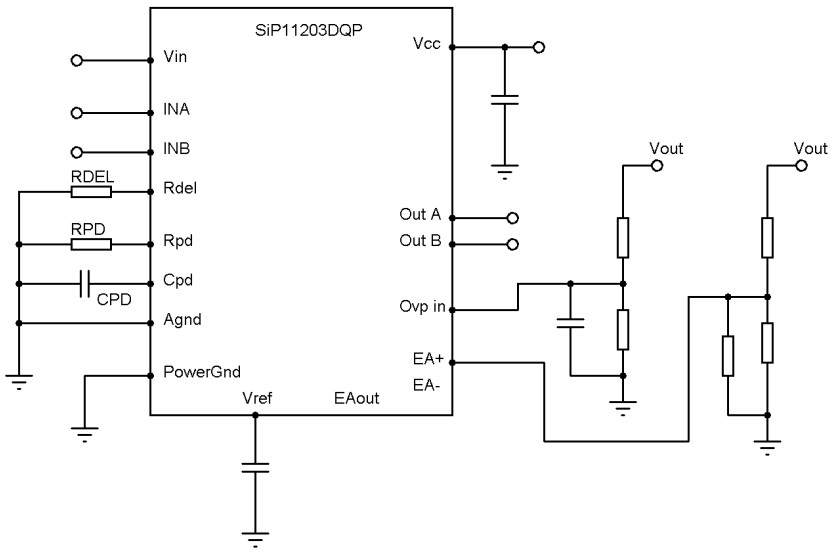



**Figure 12. Schematic showing application circuit of intelligent driver.**

## References

1. High efficiency half bridge dc to dc converter with secondary synchronous rectification. Jess Brown, Richard Davies, Dilwyn Williams and Jerry Bernacchi, PCIM 2001, Nuremberg, Germany.

2.Si9122 datasheet. http://www.vishay.com/docs/71815/71815.pdf

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